EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	30532	("IO" "I/O") with (pad or buffer)	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/18 14:35
L2	21727	("IO" "I/O") with (buffer)	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/18 14:34
L3	72779	("IO" "I/O") with (pad port pin terminal)	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/18 14:35
L4	10043	L2 and L3	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/18 14:35
L5	217116	(Power near5 (distribution analysis calculat$4 estimat$4 determin$3))	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/18 15:28
L6	1058	L4 and L5	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/18 14:37
L7	129223	(voltage "IR") adj drop	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/18 15:30
L8	225	L6 and L7	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/18 14:37

EAST Search History

L9	210	L8 and Power with (pad port pin terminal)	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/18 14:38
L10	85	L8 and Power with L2	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/18 14:38
L11	82	L9 and L10	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/18 14:39
L12	67	L11 and (wire wiring interconnect) with (resistance impedance)	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/18 15:29
L13	63	L12 and (calculat$3 determin$4) with current	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/18 15:15
L14	17	L8 and 365/226-229.ccls.	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/18 15:26
L16	422	((input$ouput "IO" "I$O") adj2 buffer)	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/18 15:28
L17	1952	((input$ouput "IO" "I$O") adj2 (pad port pin terminal))	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/18 15:31

EAST Search History

L18	115	L16 and L17	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/18 15:28
L19	223549	(Power near5 (distribution analy$5 calculat$4 estimat$4 determin$3))	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/18 15:28
L20	185413	(wire wiring interconnect conductor) with (resistance impedance)	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/18 15:29
L21	9753	L19 and L20	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/18 15:29
L22	1	L18 and L21	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/18 15:29
L23	447	power same ((input$ouput "IO" "I$O") adj2 (pad port pin terminal))	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/18 15:31
L24	0	L18 and "L25"	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/18 15:31
L25	26	L18 and L23	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/18 15:31

EAST Search History

L26	21	("20010010408" | "20010010471" | "20010011768" | "20010011771" | "20020109240" | "20020191383" | "5286656" | "5543958" | "5895967" | "5942766" | "6008533" | "6130484" | "6207548" | "6319750" | "6365978" | "6372409" | "6477046" | "6518787" | "6638793" | "6642064" | "6747349").PN. OR ("7122456").URPN.	US-PGPUB; USPAT; USOCR	OR	ON	2007/03/18 15:35
L27	14	("5220210" | "5381307" | "5567655" | "5641978" | "5675179" | "5818114" | "6008532" | "6057169" | "6078505" | "6214638" | "6222213" | "6251768").PN. OR ("6638793").URPN.	US-PGPUB; USPAT; USOCR	OR	ON	2007/03/18 15:42
L28	16	("4745305" | "5155065").PN. OR ("6057169").URPN.	US-PGPUB; USPAT; USOCR	OR	ON	2007/03/18 15:44
L29	23	("4825107" | "4947233" | "4988636" | "5045913" | "5063429" | "5239465" | "5404033" | "5552333" | "5633807" | "5654898" | "5737236" | "5764533" | "5946477" | "5987086" | "6013924" | "6057169" | "6127208" | "6385761" | "6446250").PN. OR ("6550047"). URPN.	US-PGPUB; USPAT; USOCR	OR	ON	2007/03/18 16:00
L30	7	(adding add$3 addition) with ((input$ouput "IO" "I$O") adj2 (pad port pin terminal cell)) same buffer	US-PGPUB; USPAT; USOCR	OR	ON	2007/03/18 16:02
L31	160	(adding add$3 addition) with ((input$ouput "IO" "I$O") adj2 (pad port pin terminal cell))	US-PGPUB; USPAT; USOCR	OR	ON	2007/03/18 16:02
L32	248	(adding add$3 addition) with ((input$ouput "IO" "I/O") adj2 (pad port pin terminal cell)) same buffer	US-PGPUB; USPAT; USOCR	OR	ON	2007/03/18 16:04
L33	1	L21 and L32	US-PGPUB; USPAT; USOCR	OR	ON	2007/03/18 16:03
L34	2	L18 and L32	US-PGPUB; USPAT; USOCR	OR	ON	2007/03/18 16:03
L35	106	(adding add$3) with ((input$ouput "IO" "I/O") adj2 (pad port pin terminal cell)) same buffer	US-PGPUB; USPAT; USOCR	OR	ON	2007/03/18 16:06
L36	138	(adding add$3 insert$3) with ((input$ouput "IO" "I/O") adj2 (pad port pin terminal cell)) same buffer	US-PGPUB; USPAT; USOCR	OR	ON	2007/03/18 16:04

EAST Search History

L37	27	L5 and L36	US-PGPUB; USPAT; USOCR	OR	ON	2007/03/18 16:04
L38	26	L36 and (716/1,2,4,5,11-15.ccls. 365/226.ccls. 438/14-15.ccls. 702/57,64.ccls. 703/1,2,18.ccls.)	US-PGPUB; USPAT; USOCR	OR	ON	2007/03/18 16:08
L39	10	("20020184607" | "5513119" | "5946477" | "6367051" | "6367060" | "6681373" | "6701505" | "6701506" | "6732343" | "6754877").PN. OR ("6948138"). URPN.	US-PGPUB; USPAT; USOCR	OR	ON	2007/03/18 16:14

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VLSI Circuits, 2004. Digest of Technical Papers. 2004 Symposium on
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2. **IP for embedded robustness**
Nicolaidis, M.;
Design, Automation and Test in Europe Conference and Exhibition, 2002. Proceedings
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Farbarik, R.; Xiaowen Liu; Rossman, M.; Parakh, P.; Basso, T.; Brown, R.;
Multi-Chip Module Conference, 1997. MCMC '97., 1997 IEEE
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4. **Performance evaluation of optical systems for multistage interconnection networks**
Guizani, M.;
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5. **NePSim: a network processor simulator with a power evaluation framework**
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Micro, IEEE
Volume 24, Issue 5, Sept.-Oct. 2004 Page(s):34 - 44
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» Key

IEEE JNL	IEEE Journal or Magazine
IET JNL	IET Journal or Magazine
IEEE CNF	IEEE Conference Proceeding
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Hiraki, M.; Bajwa, R.S.; Kojima, H.; Gorny, D.J.; Nitta, K.; Shri, A.;
Low Power Electronics and Design, 1996., International Symposium on
12-14 Aug. 1996 Page(s):353 - 358
Digital Object Identifier 10.1109/LPE.1996.547538
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7. **Improved linear systolic array for fast modular exponentiation**
Walter, C.D.;
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8. **Analysis of power consumption in VLSI global interconnects**
Youngsoo Shin; Hyung-Ock Kim;
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Juang-Ying Chueh; Ziesler, C.H.; Papaefthymiou, M.C.;
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Musoll, E.;
Microarchitecture, 1999. MICRO-32. Proceedings. 32nd Annual International Symposium on
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